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EPI-2818

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| First Named Inventor | Christopher S. Johnson | TRANSMITTAL FORM UNDER 37 CFR 1.10 (LARGE ENTITY) |
| Serial No. | 10/073,543 | |
| Filing Date | February 11, 2002 | |
| Group Art Unit | 2818 | |
| Examiner Name | Thong Quoc Le | |
| Confirmation No. | 5205 | |
| Attorney Docket No. | 400.149US01 | |
| Title: USER SELECTABLE BANK FOR DRAM | | |

Mail Stop: Non-Fee Amendment
Commissioner for Patents
P. O. Box 1450
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| Enclosures | | | | | |
| The following documents are enclosed: <input checked="" type="checkbox"/> An amendment and response to Office Action of May 19, 2003 (7 pgs.); <input checked="" type="checkbox"/> A return postcard. Please charge any additional fees or credit any overpayments to Deposit Account No. 501373. CUSTOMER NO. 27073 Attorneys for Applicant Leffert Jay & Polglaze, P.A. P.O. Box 581009 Minneapolis, MN 55458-1009 T - 612/312-2200 F - 612/312-2250 | | | | | |
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| Certificate of Mailing | | | | | |
| Express Mail" mailing label number: EV324608519US Date of Deposit: <u>August 19, 2003</u> These papers and fees are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and addressed to: Mail Stop NON-FEE AMENDMENT, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450. (LARGE ENTITY TRANSMITTAL UNDER 37 C.F.R. 1.10) | | | | | |



S/N 10/073,543

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named

Inventor: Christopher S. Johnson

Examiner: Thong Quoc Le

Serial No.: 10/073,543

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AMENDMENT AND RESPONSE

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In response to the Office Action dated May 19, 2003, please amend the above-identified patent application as follows:

IN THE CLAIMS

1. (Original) A memory device comprising:
an array of memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of memory cells;
a mode register; and
address circuitry coupled to the mode register to configure the addressable banks in response to a program state of the mode register.
2. (Original) The memory device of claim 1 wherein the addressable banks can be configured as either four or eight banks.
3. (Original) The memory device of claim 1 wherein the address circuitry selectively routes address signal to either a row decoder or a bank decoder in response to the mode register.
4. (Original) A dynamic random access memory comprising:
an array of X memory cells;